REMARKS

Reconsideration and allowance of the above-identified application is respectfully requested.

Claims 23 and 24 have been allowed. Claims 6 and 18-21 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. In particular, the Examiner alleges that there appears to be a lack of antecedent basis for "said controller" in claim 6. In claim 18, the Examiner questions what is meant by the phrase "and to re-close said first and second contact sets after a pre-determined period of time after verifying that said first and second contact sets have re-closed". Claims 19-21 depend from claim 18 and are rejected as well. As discussed in greater detail below, Applicant believes that the above-editorial amendments to claims 6 and 18 overcome these rejections.

Claims 1-4, 6-9, 11-14 and 22 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,052,266 to Aromin (the Aromin patent), and claims 5 and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Aromin. Further, claim 10 is rejected under 35 U.S.C. §103(a) as being unpatentable over the Aromin patent in view of U.S. Patent No. 5,936,817 to Matsko et al. (the Matsko patent). Claims 16 and 17 are objected to as being dependent upon a rejected base claim (but would otherwise be allowable if rewritten to include all the limitations of the base claim and any intervening claims), and claims 18-21 are allowable if rewritten or amended to overcome the rejection under 35 U.S.C. §112. These rejections and objections are respectfully traversed.

Specifically, Applicant respectfully submits that the Aromin and Matsko patents, either individually or in combination, fail to teach or suggest the specific features of the embodiments of the invention of a digital fault test interrupter with self-test capabilities, as specifically claimed in claims 1-24.

In particular, Applicant submits that the Aromin patent fails to teach or suggest all of the features recited in amended independent claim 1 and particularly those of the recited first and second electronic switching devices coupled to the recited actuator. In claim 1, said first electronic switching device is recited as being adapted to energize said actuator for a selected period of time, *said second electronic switching device being adapted to energize said actuator after said first electronic switching device ceases operation*. In contrast, Aromin merely discloses a booster circuit 19 and a power supply circuit 17 that initially acts concurrently before the booster circuit 19 drops out of operation. Further, the booster and power supply circuits 19 and 17 of Aromin are passive devices and not switching devices as claimed.

Applicant also submits that the Aromin patent fails to teach or suggest all of the features recited in independent claim 7 such as a processing device coupled to an output of a fault sensing circuit for receiving a fault signal and for operating first and second contact sets to open respective first and second conductive paths. Rather, Aromin teaches the use of an SCR coupled to the fault sensing circuit to drive the relay that opens the contacts. An SCR is merely an electronic switch, and not a processing device. This same reasoning applies to independent claim 11.

Applicant further submits that the Aromin patent fails to teach or suggest all the features recited in amended independent claim 22 such as energizing an actuator with a

first level of a drive current *for a selected period of time* to cause contacts to move from one of an open state or a closed state to the opposite state, and *after said selected period of time, energizing said actuator with a second level of drive current* less than said first level of said drive current to maintain said contacts in said opposite state. Rather, Aromin teaches the concurrent activation of booster and power supply circuits 19 and 17, which are concurrently applying current to solenoid SOL1. Therefore, Aromin does not disclose or suggest a first switching circuit that is activated for a selected period of time, before a second switching circuit supplies current to the solenoid.

Furthermore, Applicant submits that Aromin fails to teach or suggest the feature recited in claim 5 of the first and second switching devices being transistors. Applicant disagrees that it would have been obvious to substitute a transistor for the diodes of Aromin. Applicant also submits that the Aromin fails to teach or suggest the feature recited in claim 15 of one of the input signals comprising a load voltage signal. Applicant also disagrees that it would have been obvious to offer load voltage as an input to the ground chip as a means to offer more information about the system to the protection circuitry.

These rejections will now be discussed in more detail.

The present invention relates to a fault interrupting device, such as a ground fault circuit interrupter or an arc fault circuit interrupter. More particularly, a first embodiment of the fault interrupter comprises first and second input terminals for connection to line and neutral terminals, respectively, of a power source, first and second output terminals for connection to the line and neutral terminals, respectively, of a load, and first and second conductive paths extending between the first and second input terminals and the

first and second output terminals. The first embodiment of the fault interrupter further comprises first and second contact sets for completing and interrupting the first and second conductive paths, respectively, an actuator for operating the first and second contact sets, and a first and second electronic switching devices coupled to the actuator, wherein the first electronic switching device is adapted to energize the actuator for a selected period of time, and the second electronic switching device is adapted to energize the actuator after the first electronic switching device ceases operation.

A second embodiment of the fault interrupter comprises first and second input terminals for connection to the line and neutral terminals, respectively, of a power source, first and second output terminals for connection to the line and neutral terminals, respectively, of a load, first and second conductive paths extending between the first and second input terminals and the first and second output terminals, and first and second contact sets for completing and interrupting the first and second conductive paths, respectively. The second embodiment of the fault interrupter further comprises a fault sensing circuit adapted to produce a fault signal in response to the detection of a fault condition at the load, and a processing device coupled to an output of the fault sensing circuit for receiving the fault signal and for operating the first and second contact sets to open the respective first and second conductive paths.

A third embodiment of the fault interrupter comprises first and second input terminals for connection to the line and neutral terminals, respectively, of a power source, first and second output terminals for connection to the line and neutral terminals, respectively, of a load, and first and second conductive paths extending between the first and second input terminals and the first and second output terminals. The third embodiment of the fault interrupter further comprises first and second contact sets for

completing and interrupting the first and second conductive paths, respectively, and a processing device for operating the first and second contact sets in response to a plurality of input signals, wherein a single input of said processing device is adapted to receive more than one of said input signals.

A fourth embodiment of the fault interrupter comprises first and second input terminals for connection to the line and neutral terminals, respectively, of a power source, first and second output terminals for connection to the line and neutral terminals, respectively, of a load, and first and second conductive paths extending between the first and second input terminals and the first and second output terminals. The fourth embodiment of the fault interrupter further comprises first and second contact sets for completing and interrupting the first and second conductive paths, respectively, and a controller for operating the first and second contact sets in response to the detection of a fault condition at the load. The controller is operative to periodically open the first and second contact sets, to monitor a voltage at the load to verify that the first and second contact sets have opened, and to re-close the first and second contact sets after a predetermined period of time after verifying that the first and second contact sets have re-closed. The predetermined period of time can be extended by the controller if the first and second contact sets have not re-closed within the predetermined period of time.

Concerning the rejections under 35 U.S.C. §112, second paragraph, Applicant respectfully submits that claims 6 and 18 are amended to comport with the written description and figures. For example, the amendment of claim 6 is clearly supported by Fig. 3. The amendment to claim 18 is supported by paragraphs 32 and 33 of the specification.

In view of the amendments to claims 6 and 18, Applicant respectfully requests that the §112, second paragraph rejections be withdrawn.

In regard to the rejection under 35 U.S.C. §102(b), Aromin discloses a ground fault circuit interrupter (GFCI) that interrupts the flow of current through a pair of lines (see Fig. 1) extending between a source of power and a load. The GFCI 11 includes a circuit breaker having a switch 13 located in one of the pair of lines. The switch has a first position in which the source of power in its associated line is not connected to the load, and a second position in which the source of power in its associated line is connected to the load. A relay circuit 15 is coupled to the switch 13 for selectively positioning the switch in either the first or second position. The relay circuit includes a solenoid (SOL1) which operates in either an energized or a de-energized state. The GFCI 11 also includes a booster circuit 19 for selectively supplying a first voltage through the switch 13 and to the solenoid (SOL1) which is sufficient to cause the solenoid (SOL1) to switch from its de-energized state to its energized state. A power supply circuit 17 simultaneously supplies a second voltage to the solenoid (SOL1) which is less than the first voltage. The second voltage is sufficient to maintain the solenoid (SOL1) in its energized state after the booster circuit 19 is removed. A latch circuit operable in first and second bi-stable states allows the solenoid to switch from its de-energized state to its energized state. A fault detecting circuit detects the presence of a fault condition in at least one of the lines and causes the latch circuit to latch in its second bi-stable state upon detection of the fault condition.

The Office Action cites Aromin, Fig. 1 and col. 8, lines 14-25, as purportedly disclosing the claim 1 feature of a fault interrupter apparatus comprising an actuator (SOL1) with first (D3) and second (D1) electronic switching devices coupled to the

actuator and the first switching device being adapted to energize the actuator for a period of time and the second switching device energizes the actuator after the first switching device ceases operation. Respectfully, Applicant submits the characterization in the Office Action of what Aromin teaches or suggests is in error. Specifically, Aromin does not teach or suggest that a first electronic switching device energizes the solenoid for a selected period of time and then a second electronic device energizes the solenoid after the first ceases operation, because the booster and power supply circuits 19 and 17 in which D1 and D3 are deployed in Aromin operate concurrently. Referring to Fig. 1, and column 8, lines 14-25, it can be seen that the booster circuit 19 is selectively engaged by switches SW1 and SW2 for a certain period of time, after power is supplied to the GFCI 11. The power supply circuit 17, however, operates continuously as long as it is connected to the power supply. Power supply circuit 17 is therefore *always* in the process of energizing the solenoid SOL1, and does not energize the solenoid *after* the first switching device ceases energizing the solenoid. Therefore, since every feature of claim 1 has not been disclosed or suggested by Aromin, Aromin cannot anticipate claim 1 of the present invention, as amended herein, and it is respectfully requested that this rejection be withdrawn.

Concerning claim 7, the Office Action alleges that Aromin teaches or suggests all of the features of claim 7. Respectfully, Applicant submits that Aromin cannot teach or suggest all the features of claim 7, because Aromin does not teach or suggest the use of a processing device. Aromin teaches the use of an silicon controlled rectifier (SCR) coupled to the fault sensing circuit to drive the relay that opens the contacts. An SCR is essentially an electronic switch, and not a processing device. Therefore, since every feature of claim 7 has not been disclosed or suggested by Aromin, Aromin cannot

anticipate claim 7 of the present invention, and it is respectfully requested that this rejection be withdrawn.

In regard to claim 11, the Office Action cites Aromin as purportedly teaching or suggesting all of the features of claim 11, including a processing device for operating said first and second contact sets in response to a plurality of input signals, wherein a single input of said processing device is adapted to receive more than one of said input signals. Contrary to the Office Action, claim 11 is not anticipated by Aromin, because Aromin does not teach or suggest that U1 is considered to be able to respond to a plurality of input signals and has a single input (3) adapted to receive more than one of the input signals (one from T1 and one from T2). Pin 3 of U1 is a voltage reference pin, supplying, according to the manufacturer's data sheet (attached as appendix A), approximately 13 volts. It is therefore not a pin capable of receiving a signal from either T1 or T2. Therefore, since every feature of claim 7 has not been disclosed or suggested by Aromin, Aromin cannot anticipate claim 7 of the present invention, and it is respectfully requested that this rejection be withdrawn.

In regard to claim 22, the Office Action cites Aromin as purportedly teaching or suggesting all of the features of claim 22, including the steps of energizing said actuator with a first level of a drive current for a selected period of time to cause said contacts to move from one of an open state or a closed state to the opposite state, *and after said selected period of time*, energizing said actuator with a second level of drive current less than said first level of said drive current to maintain said contacts in said opposite state. For the same reason that claim 1 is not anticipated by Aromin, however, the method described in claim 22 cannot be anticipated by Aromin because the booster and power supply circuits 19 and 17 that energize the solenoid SOL1 of Aromin initially operate

concurrently before booster circuit 19 ceases operation. Thus, the power supply circuit 17 does not operate *after* the booster circuit 19. Therefore, since every feature of claim 22 has not been disclosed or suggested by Aromin, Aromin cannot anticipate claim 22 of the present invention, and it is respectfully requested that this rejection be withdrawn.

In regard to the rejections of claims 5 and 15 under 35 U.S.C. §103(a), Matsko discloses a circuit breaker (see Fig. 2) that includes separable contacts 44A,B,C for movement between a closed position and an open position, and an operating mechanism 42 for moving the separable contacts 44A,B,C between the closed and open positions. Current transformers 16A,B,C and potential transformers 26A,B,C sense current, voltage and frequency conditions of the separable contacts 44A,B,C and produce signals corresponding to those electrical conditions. A trip unit (microprocessors) 28, 30 employs those signals corresponding to the electrical conditions to produce a trip signal 40. A trip coil 41 employs the trip signal to actuate the operating mechanism 42 to move the separable contacts 44A,B,C to the open position. A closing mechanism produces a close signal, and a close actuator mechanism 53 employs the close signal to actuate the operating mechanism 42 to move the separable contacts 44A,B,C to the closed position. The trip unit 28, 30 includes a microprocessor-based firmware routine for selectively enabling and disabling the close actuator mechanism as a function of the signals corresponding to the electrical conditions.

Regarding the rejection of claim 5 under 35 U.S.C. §103(a), Aromin does not teach or suggest the use of transistors in the manner as claimed in claim 5, and it would not have been obvious to substitute transistors for the diodes of Aromin. While it may be true, arguably, that a transistor can be configured as a diode, this in and of itself would not anticipate nor render obvious claim 5 in view of Aromin. It would not be obvious to

use transistors in place of the diodes of Aromin because Aromin relies on the line voltages to turn on the diodes, whereas, in the present invention, and especially as claimed in claim 5, active signals are needed to induce the transistors to turn on, causing current to flow through them and applying the proper voltage to the relay. This is different from that which is taught or suggested by Aromin. Therefore, since every feature of claim 5 has not been disclosed or suggested by Aromin, and it would not have been obvious to substitute transistors for the diodes of Aromin, the rejection of claim 5 under 35 U.S.C. §103(a) is improper, and it is respectfully requested that this rejection be withdrawn.

Regarding the rejection of claim 15 under 35 U.S.C. §103(a), Aromin does not teach or suggest the use of a load voltage as an input to a processing device. Aromin does not, as discussed above, teach the use of a processing device since Aromin only teaches the use of an SCR to control the relays. Further, Aromin cannot teach the use of a load voltage as one of two inputs to the processing device as claimed in claim 15, since Aromin does not teach or suggest that the ground fault circuit interrupter can accept two signals at one of its inputs. Since the ground fault interrupter of Aromin cannot accept two signals at one of its inputs, it cannot, therefore, accept as "*one of said input signals* a load voltage signal". Therefore, since every feature of claim 15 has not been disclosed or suggested by Aromin, and it would not have been obvious to use a load voltage as one of two inputs to the processing device of Aromin, the rejection of claim 15 under 35 U.S.C. §103(a) is improper, and it is respectfully requested that this rejection be withdrawn.

In view of the above, it is believed that the application is in condition for allowance and notice to this effect is respectfully requested. Should the Examiner have any questions, kindly contact the undersigned at the number indicated below.

Respectfully submitted,

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Dated: MARCH 12, 2004

APPENDIX A
43309
Ser. No. 10/087,125

FAIRCHILD
SEMICONDUCTOR TM

www.fairchildsemi.com

RV4145A

Low Power Ground Fault Interrupter

Features

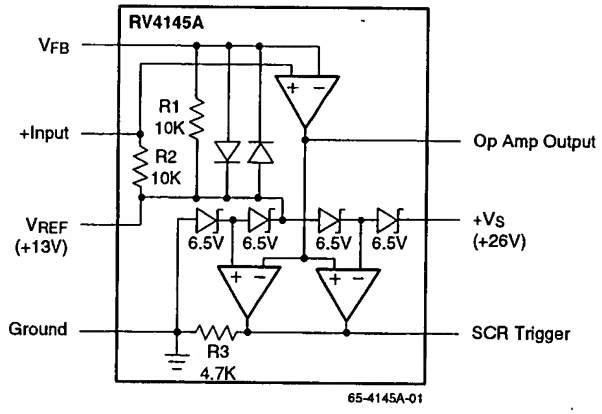
- No potentiomenter required
- Direct interface to SCR
- Supply voltage derived from AC line – 26V shunt
- Adjustable sensitivity
- Grounded neutral fault detection
- Meets U.L. 943 standards
- 450µA quiescent current
- Ideal for 120V or 220V systems

Description

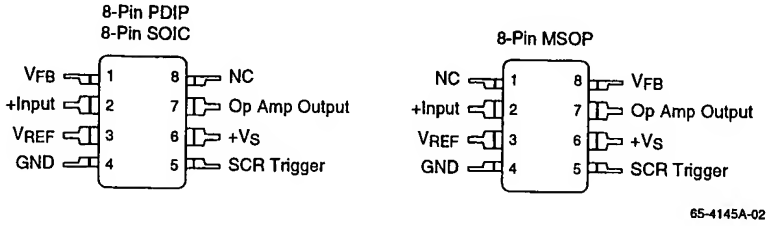
The RV4145A is a low power controller for AC outlet ground fault interrupters. These devices detect hazardous grounding conditions, such as equipment (connected to opposite phases of the AC line) in contact with a pool of water and open circuits the line before a harmful or lethal shock occurs.

Contained internally are a 26V zener shunt regulator, an op amp, and an SCR driver. WIth the addition of two sense transformers, a bridge rectifier, an SCR, a relay, and a few additional components, the RV4145A will detect and protect against both hot wire to ground and neutral wire to ground faults. The simple layout and conventional design ensure ease of application and long-term reliability.

Block Diagram



Pin Assignments



Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Current				18	mA
Internal Power Dissipation				500	mW
Storage Temperature Range		-65		+150	°C
Operating Temperature Range		-35		+85	°C
Junction Temperature				125°C	
Lead Soldering Temperature	60 Sec, DIP			300	°C
	10 Sec, SOIC, MSOP			260	°C
P_D T_A < 50°C	SOIC			300	mW
	PDIP			450	mW
	MSOP			350	mW
For T_A > 50°C Derate at	SOIC		4		mW/°C
	PDIP		6		mW/°C
	MSOP		4.7		mW/°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JA}	Thermal resistance	SOIC		240		°C/W
		PDIP		160		°C/W
		MSOP		206		°C/W

Electrical Characteristics (I_S = 1.5mA and T_A = +25°C)

Parameters	Test Conditions	Min	Typ	Max	Units
Detector Reference Voltage	Pin 7 to Pin 3	6.8	7.2	8.1	±V
Shunt Regulator					
Zener Voltage (+V_S)	Pin 6 to Pin 4	25	26	29.2	V
Reference Voltage (V_{REF})	Pin 3 to Pin 4	12.5	13	14.6	V
Quiescent Current (I_S)	+V_S = 24V		450	750	µA
Operational Amplifier					
Offset Voltage	Pin 2 to Pin 3	-3.0	0.5	+3.0	mV
+Output Voltage Swing	Pin 7 to Pin 3	6.8	7.2	8.1	V
–Output Voltage Swing	Pin 7 to Pin 3	-9.5	-11.2	-13.5	V
+Output Source Current	Pin 7 to Pin 3		650		µA
–Output Source Current	Pin 7 to Pin 3		1.0		mA
Gain Bandwidth Product	F = 50KHz	1.0	1.8		MHz
Resistors	**I_S = 0mA**				
R1	Pin 1 to Pin 3		10		kΩ
R2	Pin 2 to Pin 3		10		kΩ
R3	Pin 5 to Pin 4	3.5	4.7	5.9	kΩ
SCR Trigger Voltage	**Pin 5 to Pin 4**				
Detector On		1.5	2.8		V
Detector Off		0	1	10	mV

Electrical Characteristics (I_S = 1.5mA and -35°C ≤ T_A ≤ +85°C)

Parameters	Test Conditions	Min	Typ	Max	Units
Detector Reference Voltage	Pin 7 to Pin 3	6.5	7.2	8.3	±V
Shunt Regulator					
Zener Voltage (+V_S)	Pin 6 to Pin 4	24	26	30	V
Reference Voltage (V_{REF})	Pin 3 to Pin 4	12	13	15	V
Quiescent Current (I_S)	+V_S = 23V		500		µA
Operational Amplifier					
Offset Voltage	Pin 2 to Pin 3	-5.0	0.5	+5.0	mV
+Output Voltage Swing	Pin 7 to Pin 3	6.5	7.2	8.3	V
–Output Voltage Swing	Pin 7 to Pin 3	-9	-11.2	-14	V
Gain Bandwidth Product	F = 50KHz		1.8		MHz
Resistors	**I_S = 0mA**				
R1	Pin 1 to Pin 3		10		kΩ
R2	Pin 2 to Pin 3		10		kΩ
R3	Pin 5 to Pin 4	3.5	4.7	5.9	kΩ
SCR Trigger Voltage	**Pin 5 to Pin 4**				
Detector On		1.3	2.8		V
Detector Off		0	3	50	mV

Principles of Operation

The 26V shunt regulator voltage generated by the string of zener diodes is divided into three reference voltages: 3/4 V_S, 1/2 V_S, and 1/4 V_S. V_{REF} is at 1/2VS and is used as a reference to create an artifical ground of +13V at the op amp non-inverting input.

Figure 1 shows a three-wire 120V AC outlet GFI application using an RV4145A. Fault signals from the sense transformer are AC coupled into the input and are amplified according to the following equation:

$$V_7 = R_{SENSE} \times I_{SENSE}/N$$

Where V_7 is the RMS voltage at pin 7 relative to pin 3, R_{SENSE} is the value of the feedback resistor connected from pin 7 to pin 1, I_{SENSE} is the fault current in amps RMS and N is the turns ratio of the transformer. When V_7 exceeds plus or minus 7.2V relative to pin 3 the SCR Trigger output will go high and fire the external SCR.

The formula for V_7 is approximate because it does not include the sense transformer characteristics.

Grounded neutral fault detection is accomplished when a short or fault closes a magnetic path between the sense transformer and the grounded neutral transformer. The resultant AC coupling closes a positive feedback path around the op amp, and therefore the op amp oscillates. When the peaks of the oscillation voltage exceed the SCR trigger comparator thresholds, the SCR output will go high.

Shunt Regulator

R_{LINE} limits the current into the shunt regulator; 220V applications will require substituting a 47kΩ 2W resistor. In addition to supplying power to the IC, the shunt regulator creates internal reference voltages (see above).

Operational Amplifier

R_{SENSE} is a feedback resistor that sets gain and therefore sensitivity to normal faults. To adjust R_{SENSE}, follow this procedure: apply the desired fault current (a difference in current of 5mA is the UL 943 standard). Adjust R_{SENSE} upward until the SCR activates. A fixed resistor can be used for R_{SENSE}, since the resultant ±15% variation in sensitivity will meet UL's 943 4-6mA specification window.

The roll-off frequency is greater than the grounded neutral fault oscillation frequency, in order to preserve loop gain for oscillation (which is determined by the inductance of the 200:1 transformer and C4).

The senstivity to grounded neutral faults is adjusted by changing the frequency of oscillation. Increasing the frequency reduces the sensitivity by reducing the loop gain of the positive feedback circuit. As frequency increases, the signal becomes attenuated and the loop gain decreases. With the values shown the circuit will detect a grounded neutral fault having resistance of 2Ω or less.

The input to the op amp are protected from overvoltage by back-toback diodes.

SCR Driver

The SCR used must have a high dV/dt rating to ensure that line noise (generated by noisy appliances such as a drill motor) does not falsely trigger the SCR. Also, the SCR must have a gate drive requirement of less than 200μA. C_F is a noise filter capacitor that prevents narrow pulses from firing the SCR.

The relay solenoid used should have a 3ms or less response time in order to meet the UL 943 timing requirement.

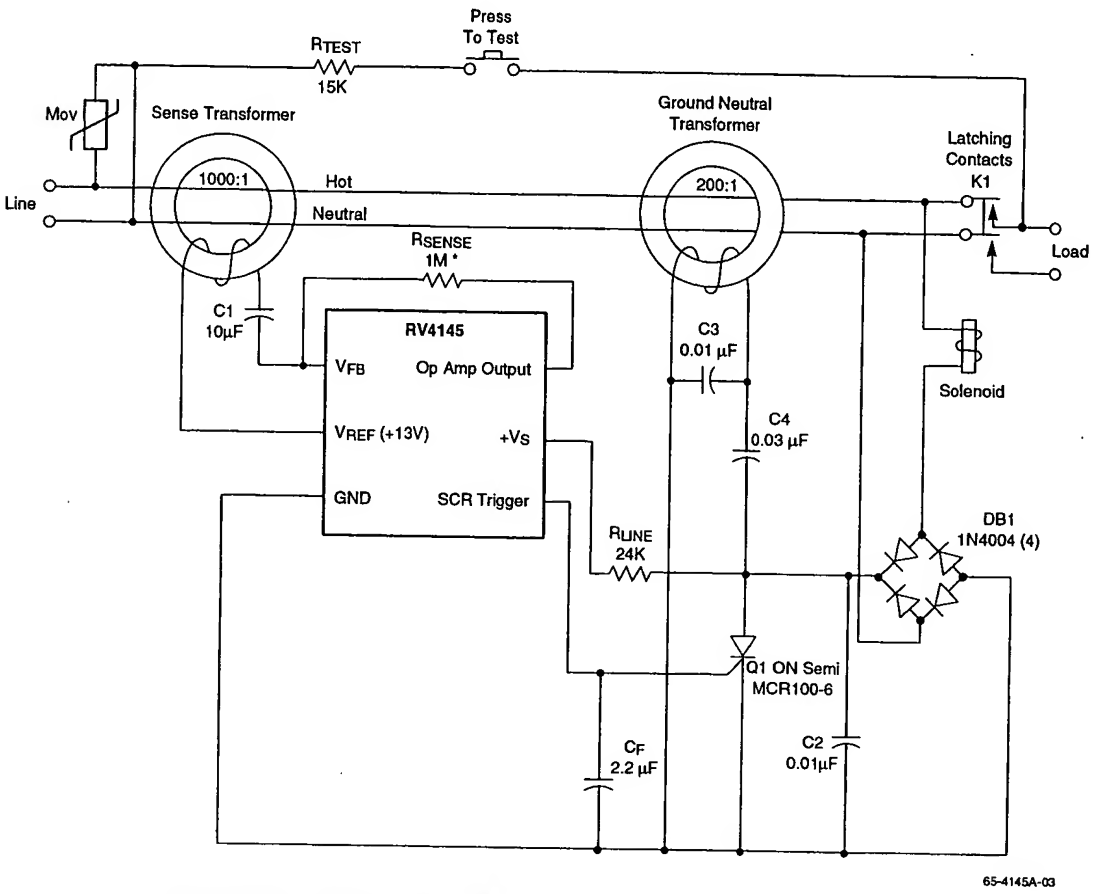
Sense Transformers and Cores

The sense and grounded neutral transformer cores are usually fabricated using high permeability laminated steel rings. Their single turn primary is created by passing the line and neutral wires through the center of its core. The secondary is usually from 200 to 1500 turns.

Magnetic Metals Corporation, Camden, NJ 08101, (609) 964-7842, and Magnetics, 900 E. Butler Road, P.O. Box 391, Butler, PA 16003, (412) 282-8282 are full line suppliers of ring cores and transformers designed specifically for GFI applications.

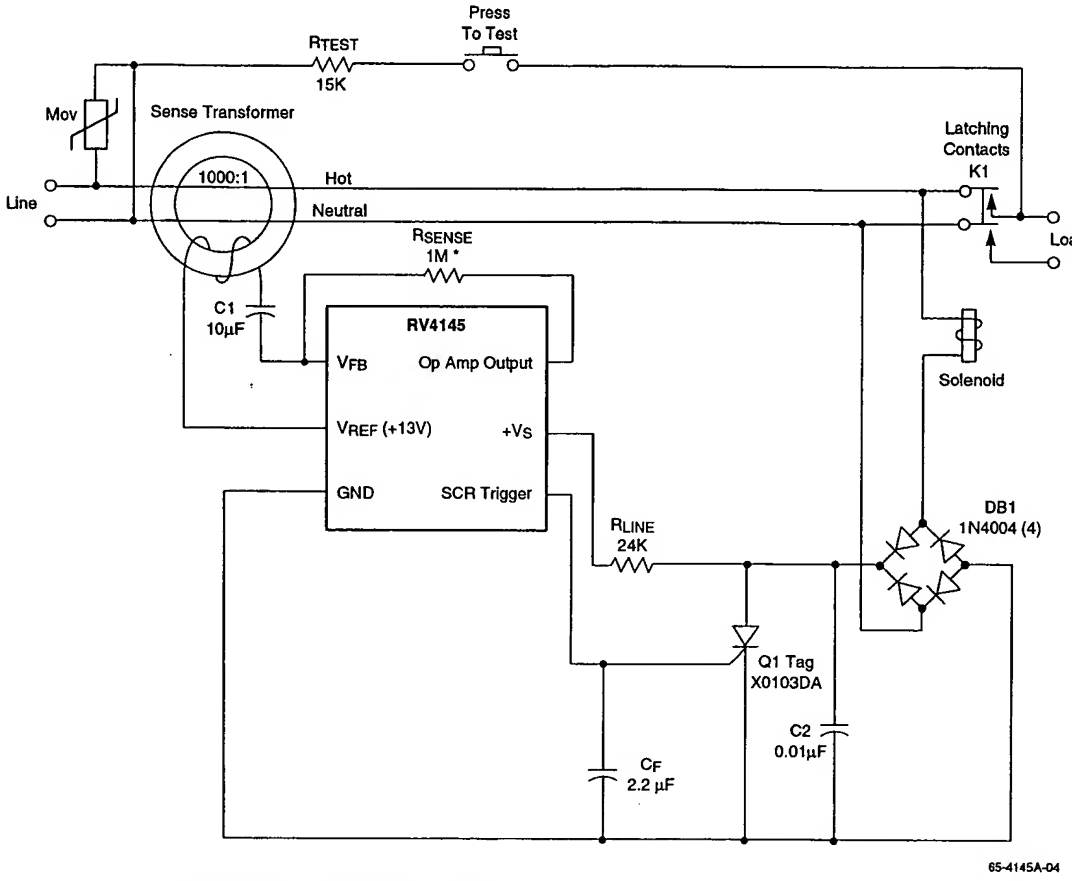
Two-Wire Application Circuit

Figure 2 shows the diagram of a 2-wire 120V AC outlet GFI circuit using an RV4145A. This circuit is not designed to detect grounded neutral faults. Thus, the grounded neutral transformer and capacitors C3 and C4 of Figure 1 are not used.



* Value depends on transformer characteristics.

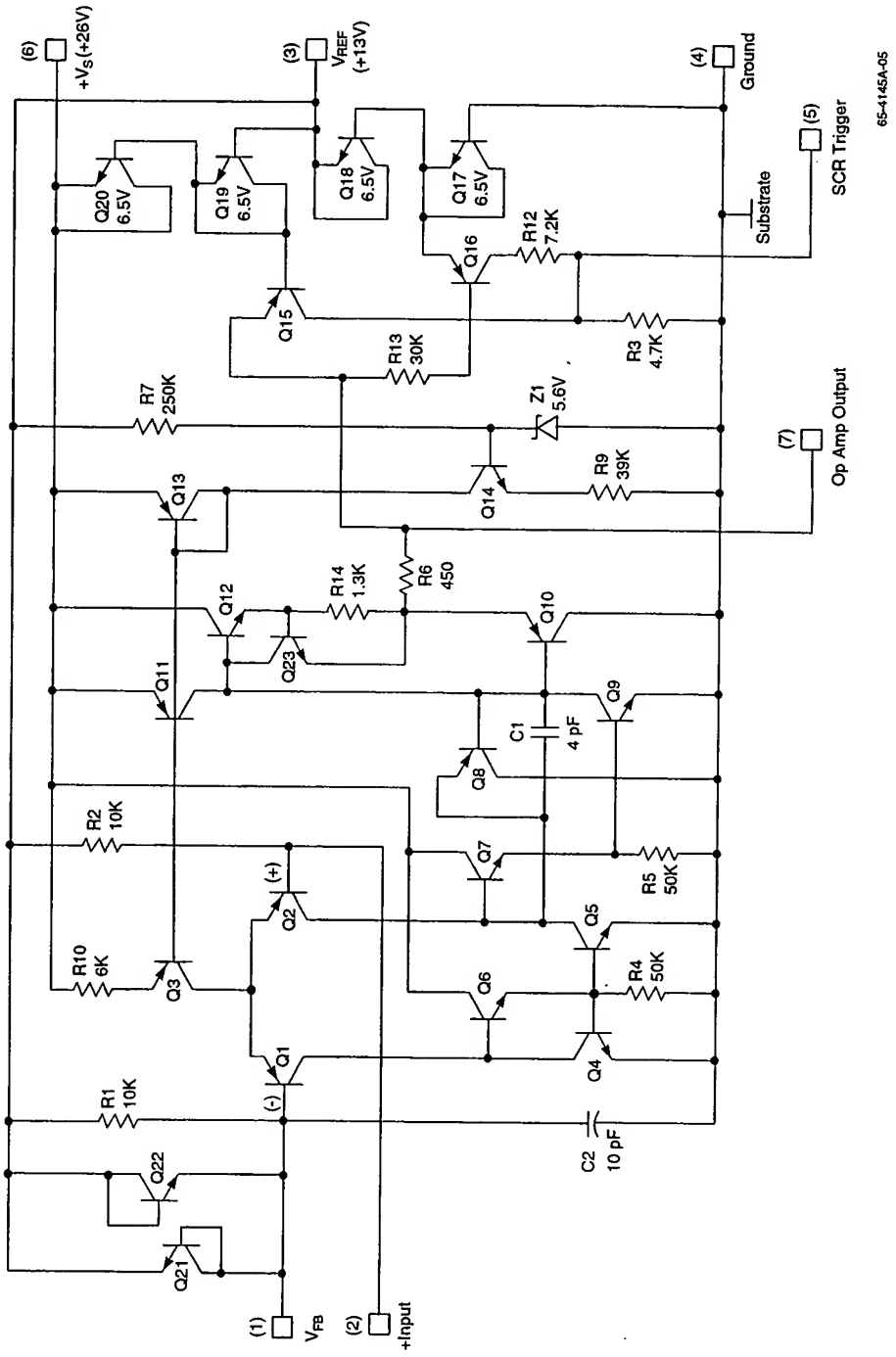
Figure 1. GFI Application Circuit (Three-Wire Outlet)



* Value depends on transformer characteristics.

Figure 2. GFI Application Circuit (Two-Wire Outlet)

Schematic Diagram



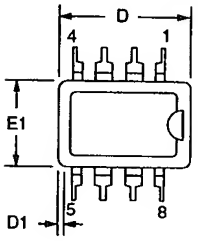
Mechanical Dimensions

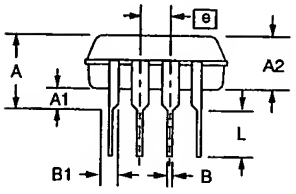
8-Lead Plastic DIP Package

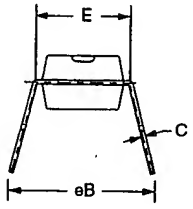
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







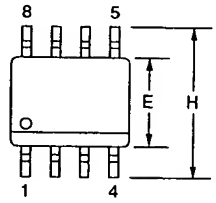
Mechanical Dimensions (continued)

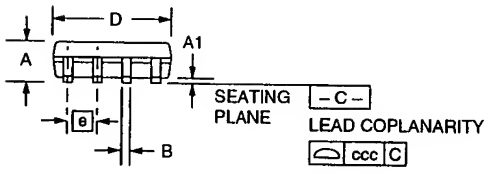
8-Lead SOIC Package

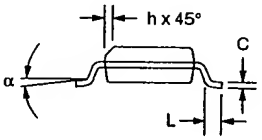
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



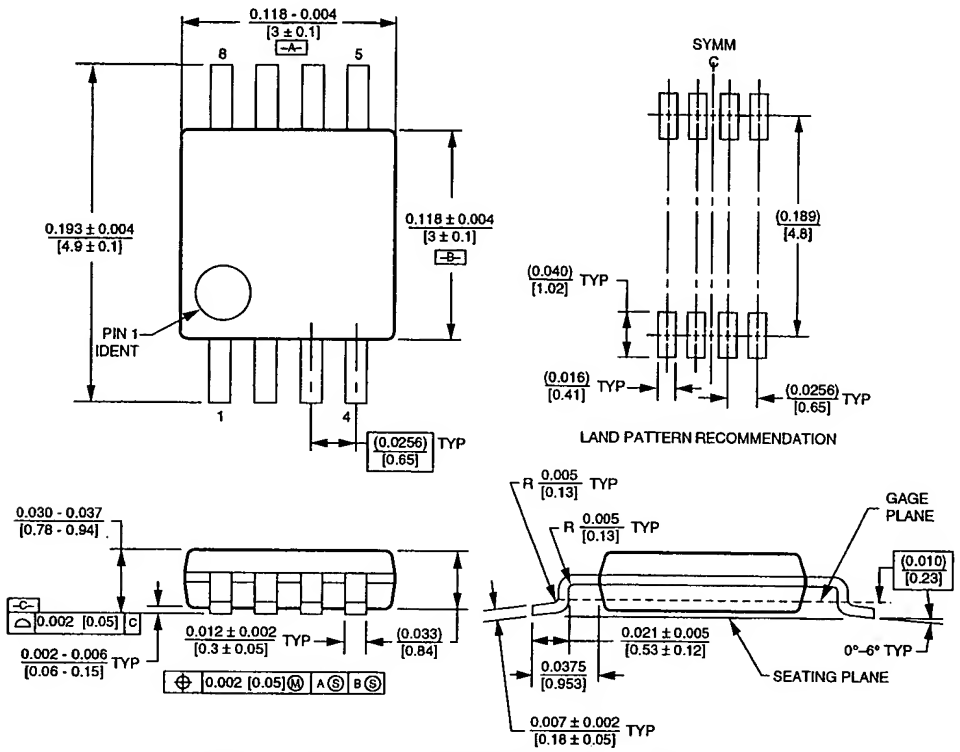




Mechanical Dimensions

8-Lead MSOP Package

Package MA08D



8-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0mm Wide
Package Number MA08D

Ordering Information

Part Number	Package	Operating Temperature Range
RV4145AN	8-Lead Plastic DIP	-35°C to +85°C
RV4145AM	8-Lead Plastic SOIC	-35°C to +85°C
RV4145AMU	8-Lead Plastic MSOP	-35°C to +85°C